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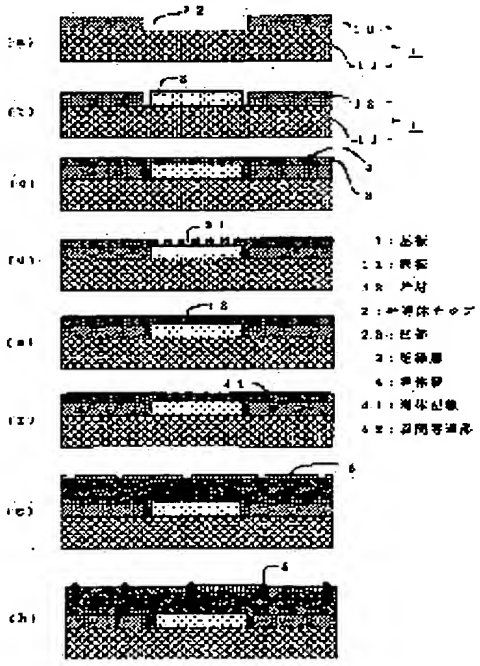
(54) SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device for enabling high density wiring and preventing peeling at the time of reflow.
SOLUTION: A substrate 1 is composed of a bottom plate 11 composed of a metal and a frame material 12 composed of a resin composite material and is provided with a recessed part 22. A semiconductor chip 2 is buried in the recessed part 22, an insulation layer 3 provided with an inter-layer conductive part 42 on the terminal of the semiconductor chip 2 is provided on it and the insulation layer 3 is provided with conductor wiring 41 in continuity with the inter-layer conductive part. Further, the insulation layer provided with a stud via and a conductor wiring pattern are laminated on the conductor wiring 41 by a build-up method.



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[Claim(s)]

[Claim 1] The substrate which has a crevice, the semiconductor chip embedded in the above-mentioned crevice, the above-mentioned semiconductor chip, and a substrate front face are covered. The insulating layer which has opening in the connection terminal area of the above-mentioned semiconductor chip, the layer flow section which gave the flow for the above-mentioned opening with the conductive ingredient, the conductor which prepares in a list at the above-mentioned insulating layer, and flows with the above-mentioned layer flow section -- with the resin composite material with which it is the semiconductor device equipped with wiring, and the above-mentioned substrate formed the thermal buyer, or the bottom plate which consists of a metal The semiconductor device characterized by having the frame material which pastes this bottom plate, has a larger through tube than the above-mentioned semiconductor chip, and consists of polyimide or resin composite material.

[Claim 2] a conductor -- the insulating layer which has on wiring stud beer which filled up the inside of beer with the conductive ingredient by the build up method, and a conductor -- the semiconductor device according to claim 1 characterized by carrying out the laminating of the wiring one by one.

[Claim 3] The semiconductor device according to claim 1 or 2 characterized by resin composite material consisting of resin, and glass fabrics, a nonwoven glass fabric, a polyamide system nonwoven fabric or a liquid crystal polymer system nonwoven fabric.

[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention relates to the semiconductor device which mounted electronic parts, such as a semiconductor chip.

[0002]

[Description of the Prior Art] Although the chip of a package and the connection of an INTAPOZA substrate containing a semi-conductor INTAPOZA substrate are conventionally made by wire bond or bump connection, a limitation is in detailed-ization of alignment precision or an electrode, and it is thought that it is difficult to deal with the pitch of 0.4mm or less.

[0003] As this cure, a high density wiring semiconductor chip is embedded by face up at a substrate, and the approach of pulling out an outer bump is indicated by the following patent official report. Namely, an external connection terminal embeds the chip prepared in the front face in a base material crevice at JP,4-25038,A. After preparing an insulating layer besides and forming a beer hall in a part for the above-mentioned external connection terminal area, it is what formed the upper circuit and the bump and formed the solder resist in the other field. As the above-mentioned base material What prepared the crevice by etching or mechanical cutting, and the thing which prepared the crevice with mechanical cutting or injection molding using thermosetting resin etc. are indicated using metals, such as aluminum.

[0004] Moreover, a semiconductor chip as well as the above-mentioned official report is embedded at JP,9-321408,A, it is what was further multilayered with the build up, and what was formed beginning to delete the above-mentioned crevice, and the pierced thing are indicated, using a stud bump as an external connection terminal of a semiconductor chip.

[0005] Moreover, using the substrate which stuck two substrates in which the through tube of the magnitude of a semiconductor chip was formed in the same part on both sides of one substrate, by embedding a semiconductor chip at the above-mentioned through tube, high density assembly is performed and the thing using copper-clad laminates, such as glass epoxy, as the above-mentioned substrate is indicated by JP,1-175297,A.

[0006]

[Problem(s) to be Solved by the Invention] However, although what sufficient leading about could not do but formed the crevice in the metal base front face as a cure against heat dissipation was used for the thing given in JP,4-25038,A since expansion of wiring was one layer, it had the technical problem that high cost started processing or exfoliation arose between a metal base and an insulating layer according to the difference of the thermal expansion of a metal base and the insulating layer prepared on this at the

time of a reflow. Moreover, although the base material which consists of resin machined resin, or injection molding of the thermoplastics was carried out and it had been obtained, high cost required the former, and bad [adhesion with the insulating layer coated from a top since the release agent is contained], since the coefficient of thermal expansion of the latter of the base material itself was large, it had the technical problem that a coefficient-of-thermal-expansion difference with a semiconductor chip is large, and a semiconductor chip broke at the time of a reflow, or it was easy to produce exfoliation between semiconductor chips. Furthermore, by the latter, the heat dissipation nature of a chip is bad and causes [of a chip] malfunction.

[0007] Since a stud bump was used for a thing given in JP,9-321408,A and it was difficult to acquire stud beer structure, it was unsuitable for wiring leading about of high density, and since the ingredient of the substrate which began to delete a crevice was not taken into consideration, the technical problem which exfoliation tends to produce that heat dissipation of a chip was inadequate occurred between semiconductor chips like the above at the time of a reflow.

[0008] Thermal conductivity is bad and the thing given in JP,1-175297,A had a technical problem in heat dissipation nature, although copper-clad laminates, such as glass epoxy, were used as the 1st and 2nd substrate (equivalent to a bottom plate and frame material).

[0009] This invention is obtained in the semiconductor device which was made in order to cancel this technical problem, and is excellent in heat dissipation nature and by which generating of the exfoliation at the time of a reflow was prevented.

[0010]

[Means for Solving the Problem] The substrate with which the 1st semiconductor device concerning this invention has a crevice, the semiconductor chip embedded in the above-mentioned crevice, The insulating layer which covers the above-mentioned semiconductor chip and a substrate front face, and has opening in the connection terminal area of the above-mentioned semiconductor chip, The above-mentioned opening is prepared in the layer flow section and the list which took the flow with the conductive ingredient at the above-mentioned insulating layer. the above-mentioned layer flow section and the flowing conductor -- with the resin composite material with which it is the semiconductor device equipped with wiring, and the above-mentioned substrate formed the thermal buyer, or the bottom plate which consists of a metal This bottom plate is pasted, and it has a larger through tube than the above-mentioned semiconductor chip, and has the frame material which consists of polyimide or resin composite material.

[0011] the 2nd semiconductor device concerning this invention -- the 1st semiconductor device of the above -- setting -- a conductor -- the insulating layer which has on wiring stud beer which filled up the inside of beer with the conductive ingredient by the build up method, and a conductor -- the laminating of the wiring is carried out one by one.

[0012] In the 1st or 2nd semiconductor device of the above, as for the 3rd semiconductor device concerning this invention, resin composite material consists of resin, and glass fabrics, a nonwoven glass fabric, a polyamide system nonwoven fabric or a liquid crystal polymer system nonwoven fabric.

[0013]

[Embodiment of the Invention] the explanatory view showing the process at which gestalt 1. drawing 1 [of operation] (a) - (h) manufactures the semiconductor device of the gestalt of operation of this invention -- it is -- the inside of drawing, and 1 -- a substrate -- it is -- from a bottom plate 11 and the frame material 12 -- becoming -- 2 -- a semiconductor chip and 22 -- a crevice and 3 -- an insulating layer and 31 -- opening and 4 -- a conductor layer and 41 -- a conductor -- as for the layer flow section and 5, wiring and 42 are [a bump and 6] solder resists.

[0014] The substrate 1 which has a crevice concerning the gestalt of operation of this invention consists of a bottom plate 11 and frame material 12, a crevice 22 is formed in a substrate 1 by the frame material 12, and the frame material 12 has a larger through tube than the semiconductor chip 2 which carries out face up of the semiconductor chip 2 to a bottom plate 11, and can lay it.

[0015] As a bottom plate 11, metals, such as copper, 42 alloys, or aluminum, or resin composite

material in which the thermal buyer was formed is used, and it is effective in excelling in heat dissipation nature. As a resinous principle of resin composite material, epoxy, poly para-phenylene system resin, or BT resin is used, and a liquid crystal polymer nonwoven fabric, a polyamide fiber nonwoven fabric, glass fabrics, or a nonwoven glass fabric is used as a reinforcement component. the thing of the through hole formed in order to miss the heat generated in the bottom plate upper part (chip mounting side) with the thermal buyer on a bottom plate background -- it is -- a bottom plate -- the through tube of 0.6mm of phi0.25 mm-phi -- a drill etc. -- opening -- the porous wall or a hole -- the whole is filled up with metal plating or a high temperature conduction ingredient. A high temperature conduction ingredient is what filled up organic resin with metal particles or a ceramic particle, and thermal conductivity is the thing of 1.0 or more W/mK. When a thermal buyer is prepared in a bottom plate using the resin composite material which stuck copper foil on the side used as the rear face, the heat which was transmitted in the thermal buyer and turned to the background gets across to the copper foil on a bottom plate background further, and radiates heat efficiently in air from there, and heat dissipation nature is further strengthened by preparing a radiation fin, a fan, etc. on copper foil. Moreover, when using for a bottom plate the resin composite material which stuck copper foil on the both sides, adhesion with frame material can be improved by removing the metal layer of the location in which a thermal buyer is formed in the location in which a semiconductor chip is prepared, and heat dissipation nature is maintained, and frame material is prepared. Moreover, when a metal is used as a bottom plate 11, while excelling in heat dissipation nature, since the coefficient-of-thermal-expansion difference with a semiconductor chip 2 is small, the exfoliation at the time of a reflow can be prevented.

[0016] Moreover, as frame material 12, coefficient of thermal expansion of a polyimide film is small, and although others, a polyimide film, or a liquid crystal polymer film is used, since adhesion with an insulating layer is good, it can prevent the exfoliation at the time of a reflow, while excelling in thermal resistance. [prepreg / above-mentioned / resin composite-material]

[0017] furthermore, the semiconductor package concerning this invention -- one side of a bottom plate -- an insulating layer and a conductor -- since wiring is stacked and it dies, a rigid high bottom plate which curvature does not generate in a back process, and a frame board are desirable to some extent, for example, when using copper for a bottom plate, the copper plate more than 0.5mm thickness is desirable, and the thickness of a frame board has good thickness and this extent of the semiconductor chip to be used.

[0018] moreover, the build up method -- an insulating layer and a conductor -- when carrying out the laminating of the wiring and giving a multilayer interconnection, by using the above-mentioned substrate concerning the gestalt of this operation, heat can be efficiently radiated outside in the heat generated from a chip, and the temperature rise of a chip is pressed down and the effectiveness of preventing malfunction and destruction of a chip is acquired.

[0019] Next, the process which manufactures the semiconductor device of the gestalt of operation of this invention is explained using drawing 1 . First, the substrate 1 which has a crevice 22 is obtained by sticking the above-mentioned frame material 12 and a bottom plate 11 { drawing 1 (a)}. A heat press or the heat laminator of lamination is desirable in respect of mass-production nature. Although lamination is possible as it is when frame material is composite prepreg, in the case of a resin film, it is necessary to use adhesives.

[0020] Next, face up of the semiconductor chip is carried out to the crevice 22 of the substrate 1 obtained as mentioned above, and it is stuck on it { drawing 1 (b)}. It is desirable to use a thermally conductive high die bond agent for attachment from a viewpoint of high heat dissipation nature. Thermally conductive high die bond material is what was high-filled up with fillers, such as copper, silver, an alumina, a diamond, silicon nitride, or boron nitride, into an epoxy resin or polyimide resin, and more than 2.0W/m and K are desirable as thermal conductivity.

[0021] Next, the insulating layer 3 of an eye is further formed from a top (drawing 1 (c)}.). Although any of liquefied resin and film resin and RCC (Resin Coated Copper) are sufficient as an insulating layer 3, the upper surface smoothness is important from a viewpoint which carries out a laminating to a

multilayer, when the point is taken into consideration, a film or RCC is desirable, drawing shows the case where RCC is used as an insulating layer, and the conductor layer 4 is stuck on the insulating layer. When an insulating layer is RCC, in the case of a film, a laminating uses a vacuum laminator using a heat press or a vacuum laminator.

[0022] { Drawing 1 (d)} which forms opening 31 (Bahia hall) in an insulating layer 3 is able to form the Bahia hall by package by exposure and development, when the insulating layer has photosensitivity, and when it does not have photosensitivity, the Bahia hall is formed using laser light. As a laser light, the higher harmonic of carbon dioxide laser, an excimer laser, and an YAG laser is desirable. The area one-shot exposure which used the mask is possible for an excimer laser, and other laser serves as a beam exposure of every one hole. Moreover, when insulator layer residue does not remain in the Bahia hall pars basilaris ossis occipitalis when the Bahia hall is formed by laser, and copper foil is not attached to an insulator layer, in order to make coppering adhesion give an insulator layer, it is necessary to give any of permanganic acid down stream processing, a plasma treatment process, or an ozone water treatment process they are after the patterning process of an insulator layer.

[0023] The obtained Bahia hall 31 is filled up with a conductive ingredient, and the layer flow section 42 is formed in it { drawing 1 (e)}. Since the layer flow section 42 is formed by filling up opening 31 with a conductive ingredient, stud beer formation is attained and the high density assembly of it becomes possible. There are an approach using coppering as an approach with which it is filled up, and an approach using a conductive paste. When RCC is used for an insulating layer, the wiring formation by plating loess is attained by filling up the Bahia hall with a conductive paste. Even when using the screen-stencil which can be printed under reduced pressure when filling up the Bahia hall with a conductive paste cannot be desirable however print under reduced pressure on account of a facility, restoration of void loess is possible by hardening under pressurization. When copper foil is not attached to an insulating layer, it is desirable at the point that the approach filled up with the Bahia hall by plating can shorten a process. Although it is necessary to use the special electrolytic plating liquid for beer philharmonic coppering plating after the usual electroless deposition to perform the Bahia hall restoration by coppering, these are marketed and are easily available. However, since thick Cu plating may be formed also in an insulator layer front face when beer is filled up with beer philharmonic coppering, it is necessary to make surface coppering thickness thin by half etching or polish if needed in that case.

[0024] next, the obtained conductor layer 4 -- the usual subtrust method -- a conductor -- { drawing 1 (f)} which forms wiring 41. Moreover, when performing detailed wiring formation, a semi ADETIBU coppering method may be applied. After this approach forms a plating resist pattern after electroless deposition formation, accumulates electrolytic plating on opening and performs wiring formation, it is for obtaining a detailed and thick copper circuit pattern by removing the electroless deposition which exfoliated the resist and remained between patterns by software etching.

[0025] further -- the insulating stratification, the Bahia hall formation, and the Bahia hall -- a conductor -- by repeating connection (or restoration) and wiring formation, multilayering of a build up wiring layer is attained, the semiconductor device of the gestalt of operation of this invention can be obtained, a solder resist 6 is further formed on an outermost layer pattern, and { drawing 1 (g)}, and the bump 5 and ball for connection are formed (drawing 1 (h)}.)

[0026]

[Example] A 405mmx340mm copper plate with an example 1. thickness of 0.5mm is used as a bottom plate 11, and silane coupling agent processing is carried out after oxide-film removal processing. Next, the substrate 1 which formed the crevice 22 is obtained by making into the frame material 12 what opened 28 holes (vertical 4 train, width 7 train) of 15mm angle in trade name:epoxy multi R-1766 and 250-micrometer thickness FR-5 {glass fabrics by Matsushita Electric Works, Ltd.} epoxy prepreg, and carrying out the press laminating of this to the above-mentioned copper plate.

[0027] After sticking a high temperature conductivity pressure sensitive adhesive sheet {trade name:T-gon2000 and the product made from the Sir magon INC} on the above-mentioned crevice 22,

the semiconductor chip 2 of 14mm angle {staggered arrangement (2025 pin(s), diameter phiof putt (copper by which surface preparation was carried out)100micrometer, and shortest pitch 370micrometer)} is stuck by pressure by face up. Next, the photosensitive dry film (it abbreviates to DF) {trade name:ViaLux and the product made from Dupont} of 68-micrometer thickness is laminated from a top with a vacuum laminator, patterning is performed using ultraviolet rays according to a part for the terminal area of a chip, and phi75-micrometer beer hall hole is formed. Next, after performing a permanganic acid process (swelling, permanganic acid processing, and reduction) and performing surface roughening of DF, a conductor layer is formed on DF at the same time it performs electroless deposition and beer philharmonic electrolytic copper plating {the product made from a trade name:cube light and Ebara You G Light} and embeds a beer hole. At this time, conductor-layer thickness was 25 micrometers. Next, after carrying out half etching of the conductor layer and setting conductor-layer thickness to 10 micrometers, the etching dry film performed patterning of a conductor layer. The diameter of a land on beer set phi100micrometer and wiring last shipment to 30 micrometers / 30 micrometers.

[0028] Surface preparation (CZ processing) {trade name:dirty bond and the MEC COMPANY LTD. make} of the wiring on the obtained substrate is carried out, the Bahia hall beer-philharmonic-plated like the last process after a lamination in the photosensitive dry film {trade name:ViaLux and the product made from Dupont} of 50-micrometer thickness and a conductor layer with a thickness of 10 micrometers are produced, and a circuit pattern is formed by etching. It accumulates one by one so that a conductor layer may turn into a total of nine layers at the same process as the following, and the solder resist which carried out opening of the terminal area to the maximum upper layer is formed. 28 semiconductor packages per substrate were obtained by finally cutting into the piece of an individual. It was 0.1-degree-C/W when the chip and bottom plate flesh-side face-to-face thermal resistance of the obtained package was measured.

[0029] 405mmx340mm 42 alloy plate with an example 2. thickness of 0.5mm was used as the bottom plate 11, and silane coupling agent processing of this was carried out. Then, 250-micrometer thickness liquid crystal polymer nonwoven fabric and epoxy prepreg which opened 28 holes (vertical 4 train, width 7 train) of 15mm angle were made into the frame material 12, the press laminating of this was carried out to the above-mentioned alloy plate, and the substrate 1 which formed the crevice 22 was obtained. a crevice 22 -- a high temperature conductivity pressure sensitive adhesive sheet -- {-- trade name: -- after sticking T-gon2000 and} made from the Sir magon INC, the semiconductor chip 2 of 14mm angle {staggered arrangement (2025 pin(s), diameter phiof putt (copper [finishing / surface preparation])100micrometer, and shortest pitch 370micrometer)} is stuck by pressure by face up.

[0030] Next, the laminating of the RCC (resin thickness of 100 micrometers, 12 micrometers of copper foil thickness) {trade name:R-0870 and the Matsushita Electric Works, Ltd. make} was carried out from the top with a heat press, patterning was performed using carbon dioxide laser according to a part for the terminal area of a chip, and phi75-micrometer beer hall hole was formed. However, in order to remove the resin residue which remained in the beer bottom after this, hole cleaning was performed with the oxygen plasma. Next, the conductive paste {trade name which contained the silver coat copper filler in the epoxy resin: Polish removed the part which embedded} made from Kyoto EREKKUSU in the beer hole using the vacuum screen printer, and was protruded after heat-hardening.

[0031] Next, the etching dry film performed patterning of a conductor layer. The diameter of a land on beer set last shipment of phi100micrometer and wiring to 30 micrometers / 30 micrometers. wiring on the obtained substrate -- melanism -- it processes and the Bahia hall and circuit pattern with which laser punching and a conductive paste were filled up with RCC of 50-micrometer thickness like the last process behind the laminating are formed by etching. It accumulates one by one so that a conductor layer may turn into a total of nine layers at the same process as the following, and the solder resist which carried out opening of the terminal area to the maximum upper layer is formed. 28 semiconductor packages per substrate were obtained by finally cutting into the piece of an individual. When the chip and bottom plate flesh-side face-to-face thermal resistance of the obtained package was

measured, it was 0.2W/degree C.

[0032] By 0.7mm in example 3. thickness, a 405mmx340mm copper plate is used as a bottom plate 11, it oxide-film-removal-processes and silane coupling agent processing of this is carried out. Thermocompression bonding was carried out to the above-mentioned bottom plate 11 by having made into the frame material 12 the plasma surface treatment finishing polyimide film with one side adhesives of 150-micrometer thickness which opened 28 holes (vertical 4 train, width 7 train) of 15mm angle, and the substrate which has a crevice was formed. a crevice -- a high temperature conductivity pressure sensitive adhesive sheet -- {-- trade name: -- after sticking T-gon2000 and} made from the Sir magon INC, the semiconductor chip 2 of 14mm angle {staggered arrangement (2025 pin(s), diameter phiof putt (surface-preparation copper)100micrometer, and shortest pitch 370micrometer)} is stuck by pressure by face up.

[0033] Next, the dry-cleaning (film DF) {trade name of 68 micrometer thickness: ViaLux and} made from Dupont were laminated from the top with the vacuum laminator, patterning was performed using ultraviolet rays according to a part for the terminal area of a chip, and the phi75micrometer beer hall hole was formed. [photosensitive] Next, after performing a permanganic acid process (swelling, permanganic acid processing, and reduction) and performing surface roughening of DF, a conductor layer is formed on DF at the same time it performs electroless deposition and beer philharmonic electrolytic copper plating {the product made from a trade name:cube light and Ebara You G Light} and embeds a beer hole. At this time, conductor-layer thickness was 25 micrometers. Next, after carrying out half etching of the conductor layer and setting conductor-layer thickness to 10 micrometers, the etching dry film performed patterning of a conductor layer. The diameter of a land on beer set last shipment of phi100micrometer and wiring to 30 micrometers / 30 micrometers. CZ processing is performed to wiring on the obtained substrate, the Bahia hall beer-philharmonic-plated like the last process after a lamination in DF {trade name:ViaLux and the product made from Dupont} of 50-micrometer thickness and a conductor layer with a thickness of 10 micrometers are produced, and a circuit pattern is formed by etching. It accumulates one by one so that a conductor layer may turn into a total of nine layers at the same process as the following, and the solder resist which carried out opening of the terminal area to the maximum upper layer is formed. 28 semiconductor packages per substrate were obtained by finally cutting into the piece of an individual. When the chip and bottom plate flesh-side face-to-face thermal resistance of the obtained package was measured, it was 0.1W/degree C.

[0034] The 405mmx340mm glass epoxy laminate {trade name which stuck copper foil of 18 micrometers of thickness on both sides by 1mm in example 4. thickness: Through-hole plating of 20-micrometer thickness is performed, and a thermal buyer hole is formed, and let this be a bottom plate 11, after DESUMIA [the part which mounts the semiconductor chip of epoxy multi and} by Matsushita Electric Works, Ltd. / four phi0.3mm through tubes / with a drill / open and] beforehand.

[0035] glass epoxy prepreg FR- of 250-micrometer thickness which opened 28 holes (vertical 4 train, width 7 train) of 15mm angle -- the press laminating was carried out to the above-mentioned bottom plate 11 by having made 4 {the Matsushita Electric Works, Ltd. make} into the frame material 12, and the substrate which has a crevice was formed. Under the present circumstances, it is in the condition that the thermal buyer hole is exposed to a crevice. the above-mentioned crevice -- a high temperature conductivity pressure sensitive adhesive sheet -- {-- trade name: -- after sticking T-gon2000 and} made from the Sir magon INC, the semiconductor chip 2 of 14mm angle {staggered arrangement (2025 pin(s), diameter phiof putt (surface-preparation copper)100micrometer, and shortest pitch 370micrometer)} is stuck by pressure by face up.

[0036] Next, photosensitive dry cleaning (film DF) {trade name:ViaLux of 68-micrometer thickness and} made from Dupont were laminated from the top with the vacuum laminator, patterning was performed using ultraviolet rays according to a part for the terminal area of a chip, and the phi75micrometer beer hall hole was formed. Next, after performing a permanganic acid process (swelling, permanganic acid processing, and reduction) and performing surface roughening of DF, a conductor layer is formed on DF at the same time it performs electroless deposition and beer

philharmonic electrolytic copper plating {the product made from a trade name:cube light and Ebara You G Light} and embeds a beer hole. Under the present circumstances, it exposes to an inferior surface of tongue, and the inside of a thermal buyer is also galvanized. At this time, conductor-layer thickness was 25 micrometers. Next, after carrying out half etching of the conductor layer and setting conductor-layer thickness to 10 micrometers, the etching dry film performed patterning of a conductor layer. The diameter of a land on beer set last shipment of 100 micrometers and wiring to 30 micrometers / 30 micrometers. CZ processing is performed to wiring on the obtained substrate, the Bahia hall beer-philharmonic-plated like the last process after a lamination in DF {trade name:ViaLux and the product made from Dupont} of 50-micrometer thickness and a conductor layer with a thickness of 10 micrometers are produced, and a circuit pattern is formed by etching. It accumulates one by one so that a conductor layer may turn into a total of nine layers at the same process as the following, and the solder resist which carried out opening of the terminal area to the maximum upper layer is formed. 28 semiconductor packages per substrate were obtained by finally cutting into the piece of an individual. When the chip and bottom plate flesh-side face-to-face thermal resistance of the obtained package was measured, it was 0.9W/degree C.

[0037] The semiconductor chip (2025 pin(s)) of 14mm angle and isomorphism-like crevice to mount were formed in 1.30mm angle of examples of a comparison, and 5mm thickness glass epoxy laminate {trade name:FR-4 and the Matsushita Electric Works make} by the mechanical cutting method, and the chip was pasted up on them by the silicone die bond agent by face up in the substrate crevice. From the top to furthermore, a photosensitive epoxy system interlayer-insulation-film {trade name: XP-9500cc and} made from SHIPUREI Far East were applied so that it might become 50 micrometers in thickness after hardening, and 90 degrees C dried for 45 minutes. According to a part for the terminal area of a chip, patterning was performed using ultraviolet rays, and phi75-micrometer beer hall hole was formed. Next, after performing the permanganic acid process (swelling, permanganic acid processing, and reduction) and performing surface roughening, when non-electrolytic copper plating and electrolytic copper plating were performed, plating was formed in the form where the beer hall configuration was met. Subsequently, copper patterning (last shipment=30micrometer / 30 micrometers) was performed by the photo etching method. Next, the multilayer interconnection was formed by the photograph beer build up method in the process same for wiring leading about. Since stat beer structure was not able to be taken at this time, a little beer of a vertical layer was shifted and the TEADO rope mold land was used. It could not let-two wiring pass but had to stop therefore, having to accumulate it a total of 17 layers among bumps. Although the package furthermore done tried DBA (direct bonding attaching) connection by the golden bump at the time of mother board connection, when it was pressurization, sedimentation of a terminal area took place, and good connection was not obtained. Moreover, when the chip and bottom plate flesh-side face-to-face thermal resistance of the obtained package is measured, it is 1.8W/degree C, and with this configuration, the heat produced from the chip was not able to be missed efficiently.

[0038] The semiconductor chip (2025 pin(s)) of 14mm angle and isomorphism-like crevice to mount were formed in 2.30mm angle of examples of a comparison, and 1mm thickness copper plate by the mechanical cutting method, and the chip was pasted up on them by the silicone die bond agent by face up in the substrate crevice. From the top to furthermore, a photosensitive epoxy system interlayer-insulation-film {trade name:} made from XP-9500cc and SHIPUREI was applied so that it might become 50 micrometers in thickness after hardening, and 90 degrees C dried for 45 minutes. According to a part for the terminal area of a chip, patterning was performed using ultraviolet rays, and the phi75micrometer beer hall hole was formed. Next, after performing the permanganic acid process (swelling, permanganic acid processing, and reduction) and performing surface roughening, when non-electrolytic copper plating and electrolytic copper plating were performed, plating was formed in the form where the beer hall configuration was met. Subsequently, copper patterning (last shipment=30micrometer / 30 micrometers) was performed by the photo etching method. Next, the multilayer interconnection was formed by the photograph beer build up method in the process same for

wiring leading about. Since stat beer structure was not able to be taken at this time, a little beer of a vertical layer was shifted and the TEADO rope mold land was used. It could not let-two wiring pass but had to stop therefore, having to accumulate it a total of 17 layers among bumps. Although the semiconductor package further done although it was good when the chip and bottom plate flesh-side face-to-face thermal resistance of the obtained package was measured tried DBA connection by the golden bump at the time of mother board connection, when it was pressurization, sedimentation of a terminal area took place, and good connection was not obtained. Moreover, when the solder reflow test of the obtained package was carried out, exfoliation occurred between the metal base section and an epoxy interlayer insulation film. Since this has many differential thermal expansions of a metal and an interlayer insulation film, and number of layerses of a build up layer, it originates in big stress having arisen.

[0039]

[Effect of the Invention] The substrate with which the 1st semiconductor device of this invention has a crevice, the semiconductor chip embedded in the above-mentioned crevice, The insulating layer which covers the above-mentioned semiconductor chip and a substrate front face, and has opening in the connection terminal area of the above-mentioned semiconductor chip, The above-mentioned opening is prepared in the layer flow section and the list which took the flow with the conductive ingredient at the above-mentioned insulating layer. the above-mentioned layer flow section and the flowing conductor -- with the resin composite material with which it is the semiconductor device equipped with wiring, and the above-mentioned substrate formed the thermal buyer, or the bottom plate which consists of a metal It has a larger through tube than the above-mentioned semiconductor chip, and it is the thing equipped with the frame material which consists of polyimide or resin composite material, excels [this bottom plate is pasted, and] in heat dissipation nature, and is effective in the ability to prevent the exfoliation at the time of a reflow.

[0040] the 2nd semiconductor device of this invention -- the 1st semiconductor device of the above -- setting -- a conductor -- the insulating layer which has on wiring stud beer which filled up the inside of beer with the conductive ingredient by the build up method, and a conductor -- it is what carried out the laminating of the wiring one by one, and is effective in high density wiring being possible.

[0041] In the 1st or 2nd semiconductor device of the above, resin composite material consists of resin, and glass fabrics, a nonwoven glass fabric, a polyamide system nonwoven fabric or a liquid crystal polymer system nonwoven fabric, the 3rd semiconductor device of this invention can prevent the exfoliation at the time of a reflow, and it is effective in excelling in thermal resistance.